FIG. 1

Figure 2a

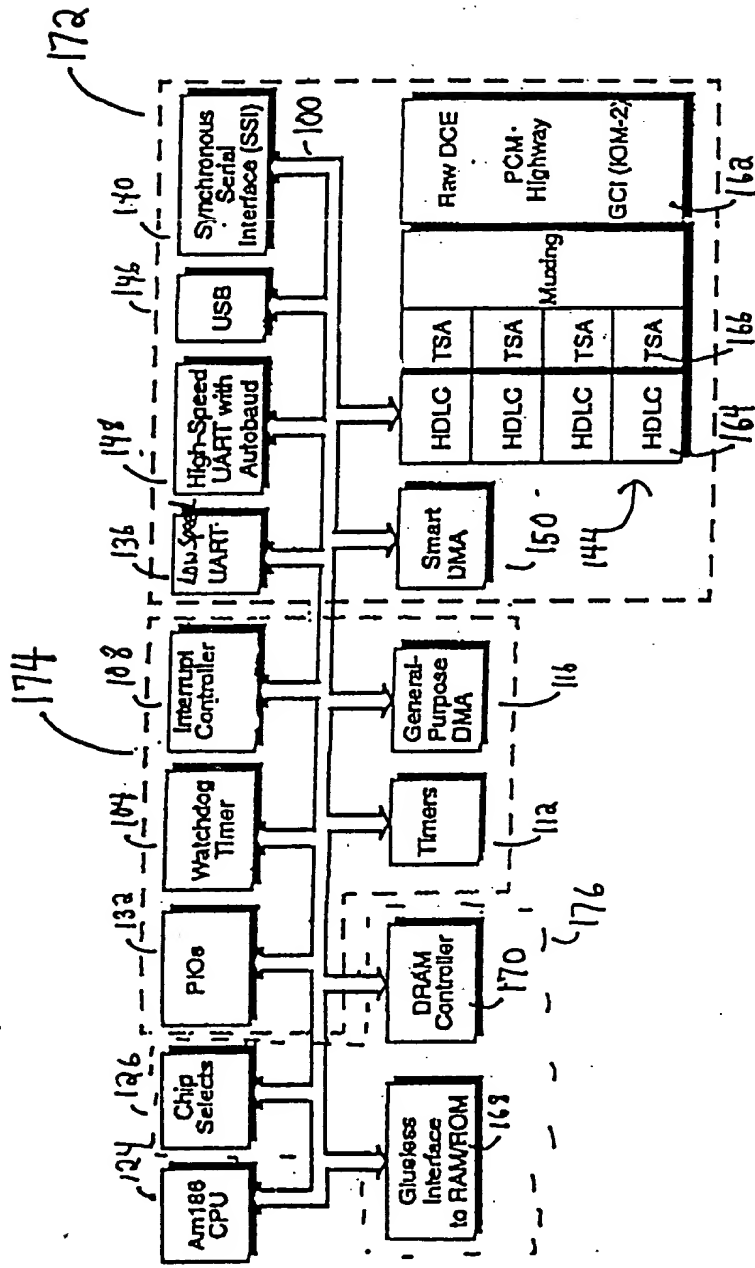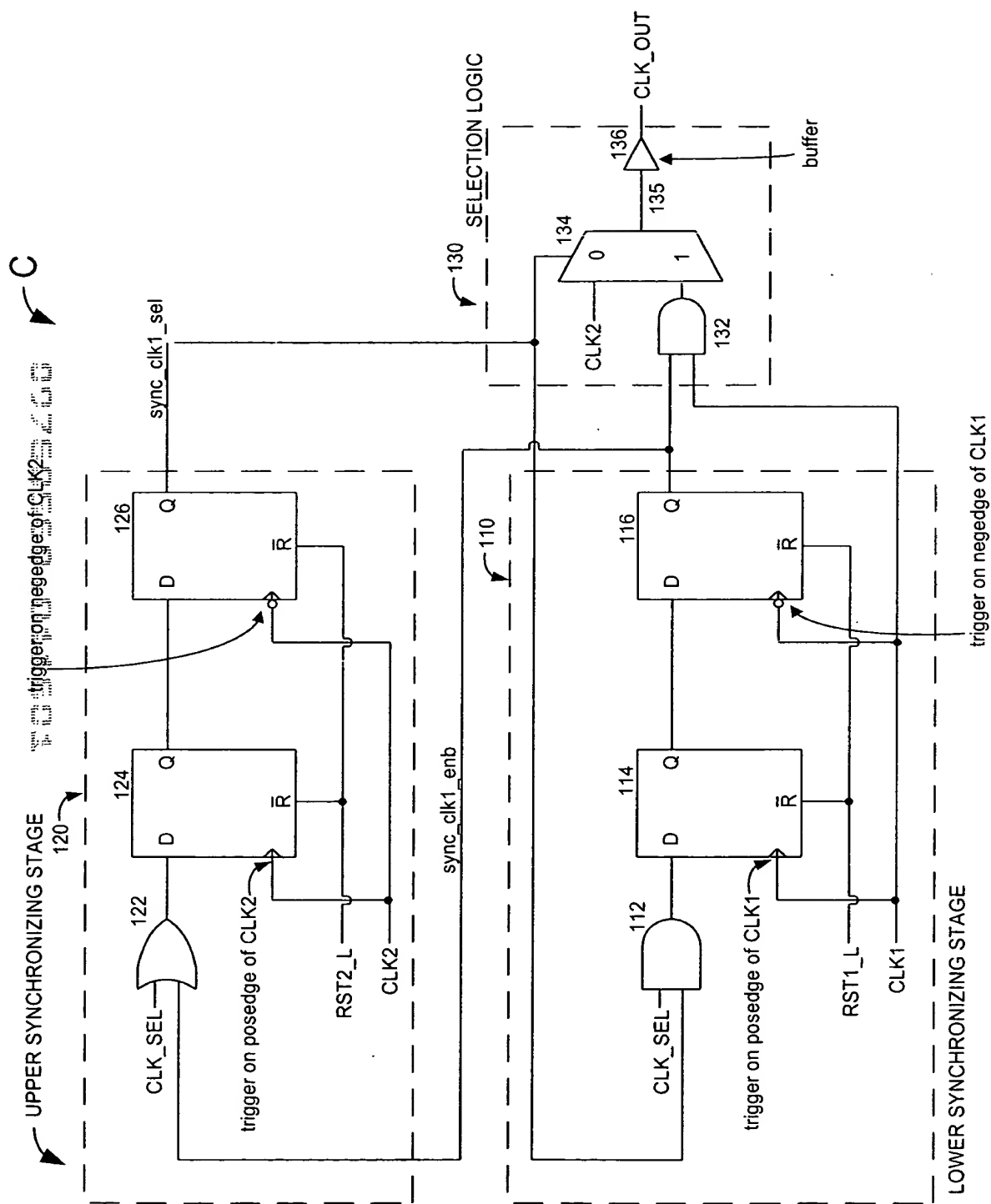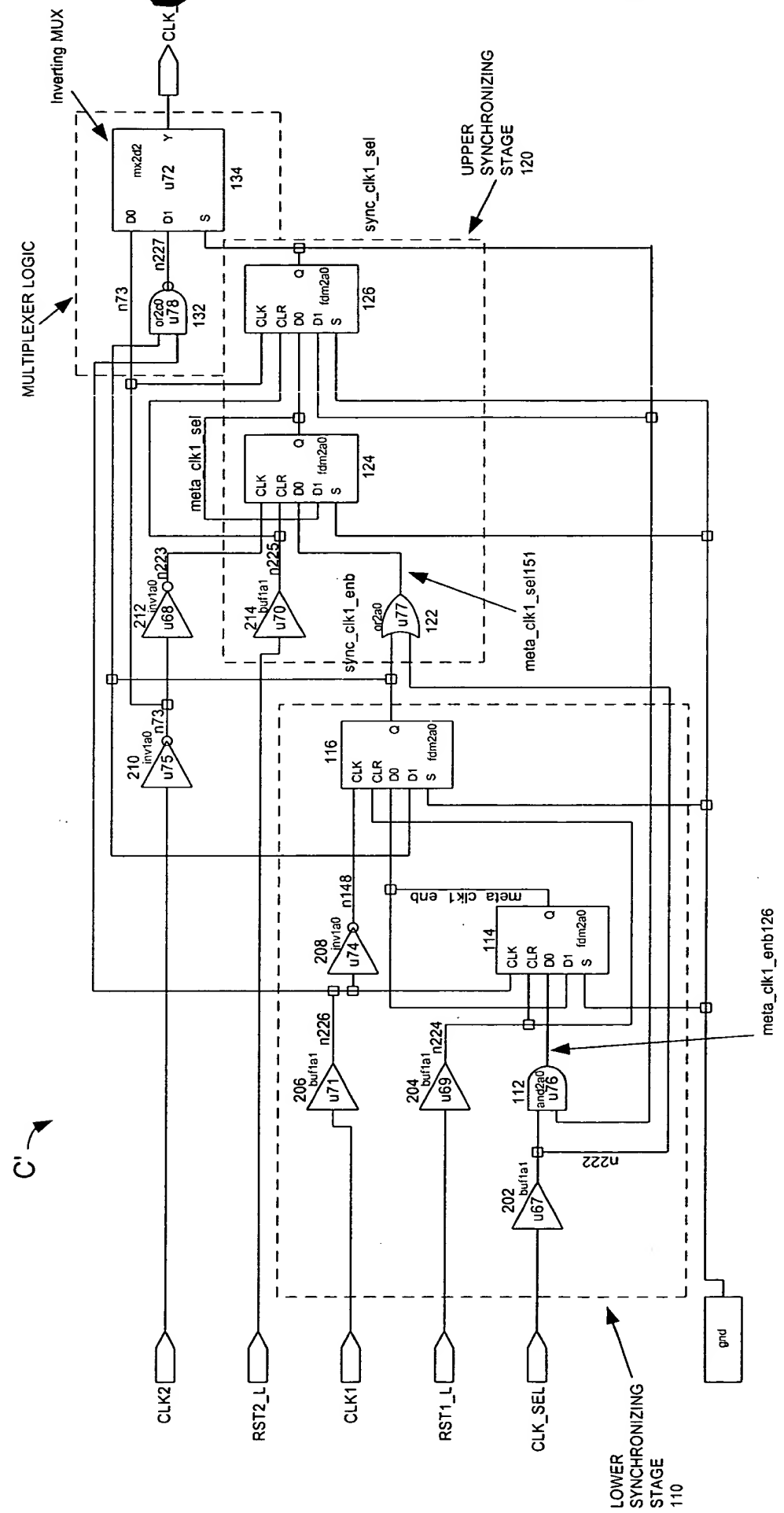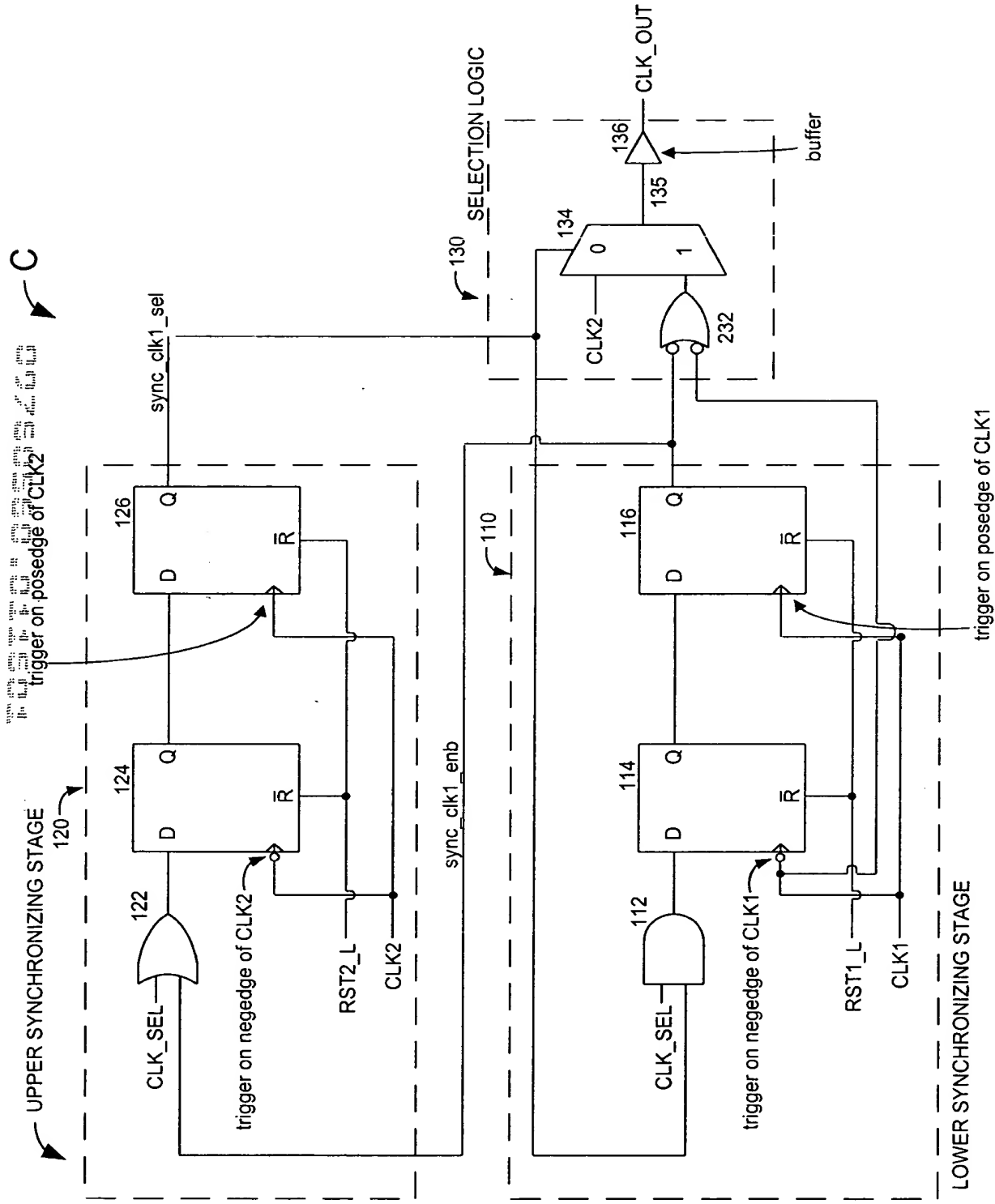Synthesized (gate implementation) schematic from Verilog RTL

Figure 2b

Figure 2c

Notes:

* RST2_L is system reset synchronized to CLK2.
* RST1_L is system reset synchronized to CLK1.
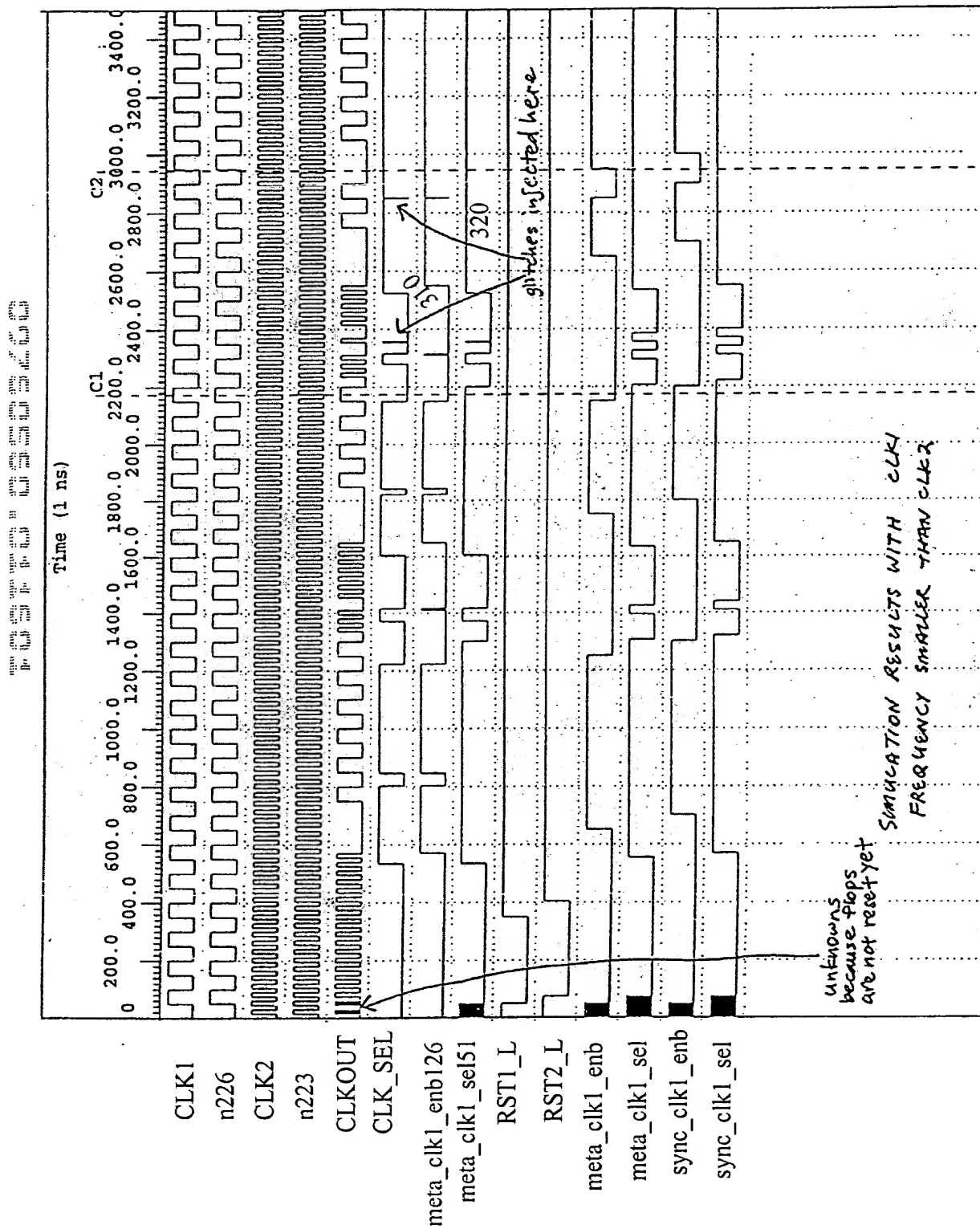* CLK_SEL is an asynchronous signal.

Figure 3

Figure 4

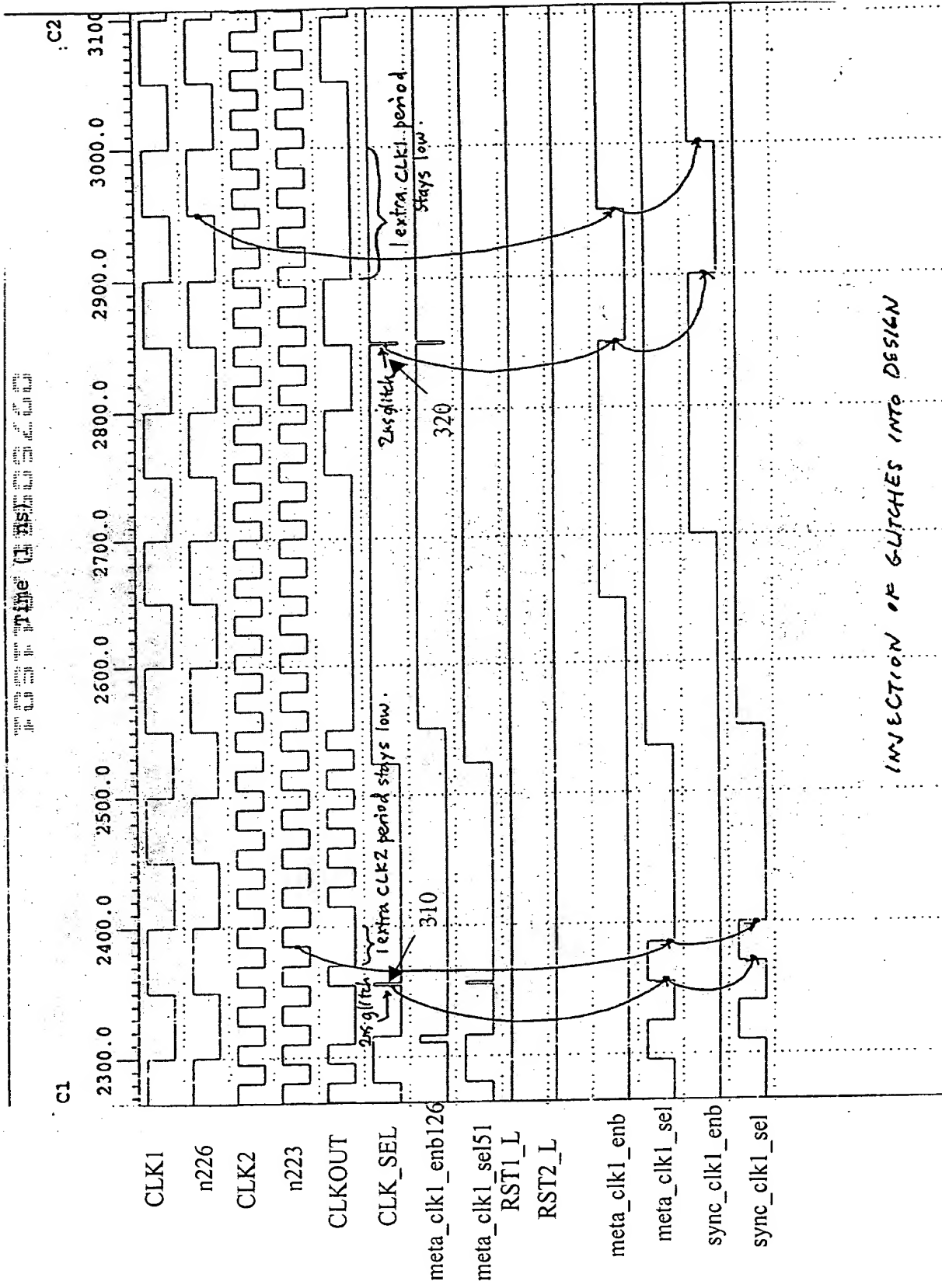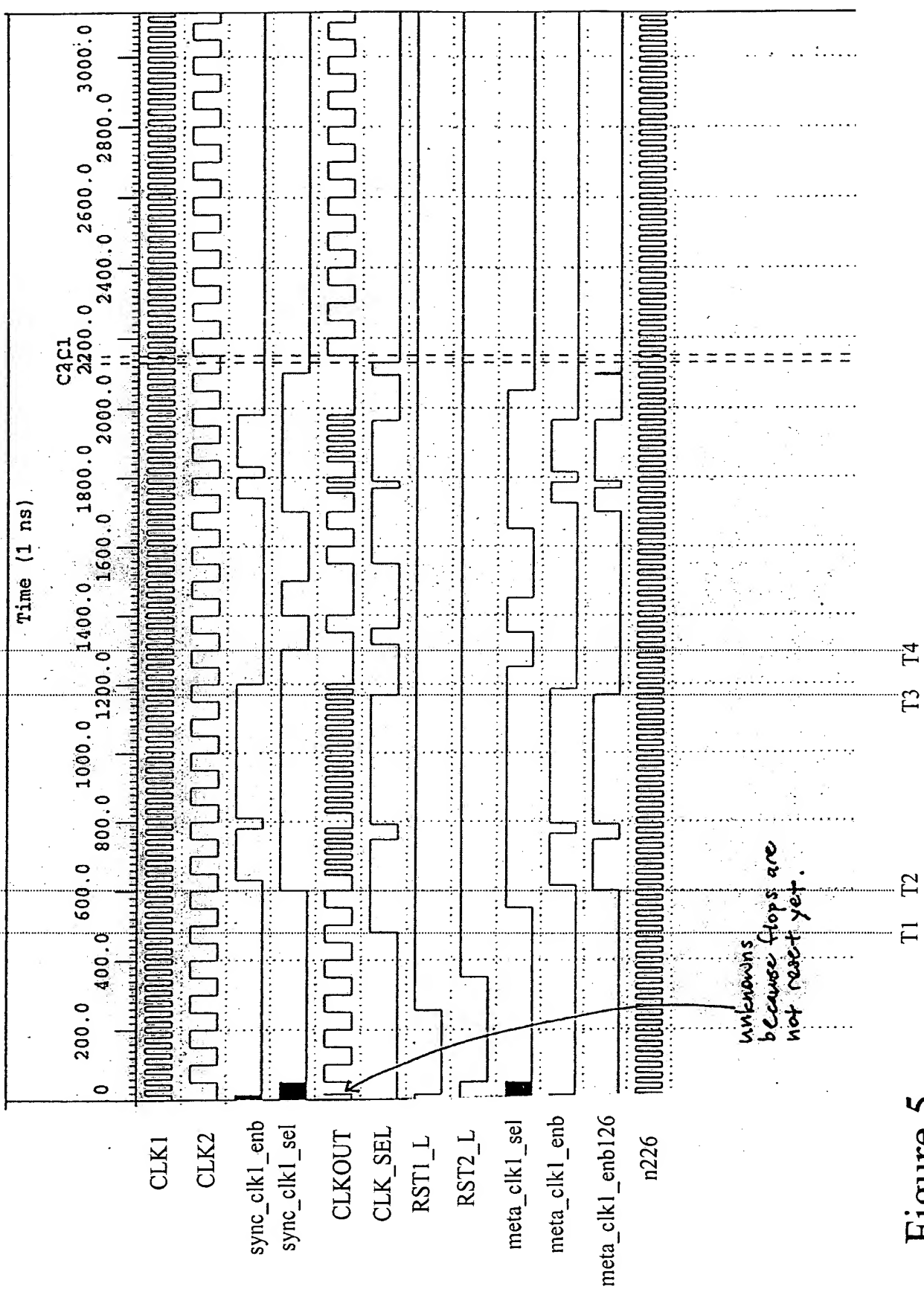INJECTION OF GLITCHES INTO DESIGN

Figure 5